## REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 3-7 have been amended. Thus, claims 1-8 are currently pending in the application and subject to examination.

In the Office Action mailed May 21, 2004 the Examiner objected to FIG. 5 and claim 3. The examiner rejected claims 3-8 under 35 U.S.C. §112, first paragraph. The Examiner further rejected claims 1-2 and 5 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,266,294 to Yada et al. (Yada). The Examiner indicated that claims 3-4 and 6-8 contain allowable subject matter. The Applicant acknowledges with gratitude the indication of allowable subject matter.

Regarding the objection to FIG. 5, a proposed corrected drawing sheet, which includes corrections to FIG. 5, is enclosed with this Response. If any additional amendment is necessary to overcome this rejection, the Examiner is requested to contact the Applicant's undersigned representative.

Regarding the objection to claim 3, this claim has been amended in accordance with the Examiner's suggestions. The Applicant therefore respectfully requests withdrawal of the objection to claim 3.

Regarding the rejection of claims 3-8 under 35 U.S.C. §112, first paragraph, claims 3-7 have been amended responsive to this rejection. The Applicant respectfully submits that the amendments to claims 3-7 overcome the rejection under 35 U.S.C. §112, first paragraph, and accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-2 and 5 stand rejected under 35 U.S.C. §102(e) as being anticipated by Yada et al. This rejection is respectfully traversed, as follows.

Yada teaches an integrated circuit device for receiving an external clock signal and a clock enable signal and for supplying to an internal circuit an internal clock signal which has a predetermined phase relationship with the external clock signal. A delay locked loop (DLL) circuit for generating a delay clock signal, synchronized and in phase with the external clock signal, is operated continuously even in a low power consumption mode, and the provision of the delay clock signal to the internal circuit is halted. As discussed in the Abstract, when the mode is switched from the low power consumption mode to the normal mode, the delay clock signal generated by the DLL circuit, which is operated continuously, is supplied as in internal clock signal to the internal circuit again. A phase comparator 23 compares the phase of a clock signal I-CLK with that of the clock signal C-CLK. As shown in Fig. 3, Yada teaches that the delay controller 24 adjusts the variable delay circuits 20, 21 in accordance with a result of comparison of the phase comparator 23. Nowhere does Yada teach or suggest the starting an increase of the delay time *at any time when a phase difference is detected* in the step of comparing.

Regarding claim 1 of the present invention, Applicant notes that Yada does not teach or suggest at least the limitations of "comparing phases of said output signal and said input signal with each other" and "starting an increase of the delay time at any time when a phase difference is detected in the step of comparing," as claimed in claim 1. Neither of these limitations is recited in the claims of Yada. Accordingly, the Applicant respectfully requests that the 102 rejection be withdrawn.

Regarding claim 5 of the present invention, Applicant notes that claim 5 recites the limitations "detecting means for detecting a phase difference between said phase of said input signal and said phase of said output signal" and "delaying means for increasing a delay time of said phase of said output signal when starting the delay time adjustment until said phase difference becomes N periods, where N is an integer other than zero." Neither of these limitations is taught or suggested by Yada. Accordingly, the Applicant respectfully requests that the §102 rejection be withdrawn.

Regarding the rejections of claims 1 and 5, the Applicant notes that both Yada and the present invention are assigned to Fujitsu Limited, of Kanagawa, Japan, the assignee of record for the present invention. As Yada is commonly owned with the present invention, any obviousness rejection under 35 U.S.C. § 103 can be overcome by making a statement of common ownership under § 35 U.S.C. § 103(c). Such a statement of common ownership is enclosed with this Response.

Claim 2 is dependent from claim 1. Claim 2 is also allowable for at least those reasons discussed above in reference to claim 1. Accordingly, withdrawal of the rejection of claim 2 is respectfully requested.

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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CMM/SES

Enclosures: Statement of Ownership
Figure 5